Applicant requests the Examiner identify the location of the phrase so that an appropriate correction to the Specification may be made.

In regard to items 5 and 6 in the Office Action, Applicant has modified the claims in order to comport with the requirement of 35 U.S.C. §112, second paragraph. Applicant submits that the modified claims are in compliance with §112 and accordingly Applicant requests that the Examiner now withdraw these rejections.

Applicant respectfully requests reconsideration of the prior art rejections that have been set forth by the Examiner under 35 U.S.C. §§102 and 103. Applicant respectfully submits that that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's presently claimed invention.

More specifically, Applicant has disclosed new and improved manufacturing techniques and the resultant corresponding structures that provide an improved ability to achieve greater semiconductor chip package density without incurring the problems inherent with previous approaches to the manufacture of similar high-density semiconductor products.

More specifically, Applicant has disclosed techniques and structures which overcome various problems including those previously encountered when grinding and dicing semiconductor chips. More specifically, in accordance with a preferred exemplary embodiment of the present invention, Applicant has discovered that improvements can be achieved by temporarily surrounding semiconductor chip members with resin and thereafter grinding and polishing surfaces of the chips and the surrounding resin such that resin remains only around the sides of the chip and thereafter a sheet that had been supporting the chip members during the grinding and polishing processing as described in Figure 1D may be removed readily without damage to the chip members. See, for example, Figures 1E-1F and the corresponding description in the Specification.

Dicing may thus readily be performed through cutting into only the resin between adjacent chip members 4 as shown in Figure 1K. This advantageously insures that no damage may be encountered by the individual chip members 4.

The prior art of record fails to provide any teaching or suggestion whatsoever regarding this advance in the art. More specifically, the Yoshikazu reference, U.S. Patent No. 5,989,982 is merely directed to a prior art technique wherein the adjacent chips are diced with cutting instrument 14, however, there is no disclosure regarding the grinding and polishing that is performed as shown in Figure 1D of this application which provides the ability to achieve improved packing density.

Yoshikazu actually relates to a much different technique wherein chips are simply separated from one another without any grinding. Thus, its structure is inherently different as it specifically describes application of resin essentially encapsulating chips members except for the sides of the chip opposite to the electrical connections. This is different than Applicant's claimed invention wherein resin is located only around the side walls of the semiconductor chip elements and specifically not on the side at which the electrical connections for the chip members are located. Yoshikazu thus actually teaches away then from the presently claimed invention.

The remaining prior art reference of record, the Tomonori, Japanese prior art reference JP 05-055278 is also directed to a much different semiconductor chip structure wherein the semiconductor chip only has resin on a surface at which the electrical connections for the chip member 2 are located. It is thus similar to Yoshikazu in this regard. This prior art structure is not only different from Applicant's claimed invention but similarly does not provide the unique advantages inherent in Applicant's claimed structure. More specifically, as noted in the Specification, individual chip members 4 are located on a sheet 5 that is preferably only temporarily secured to the chip members. Advantageously the

adhesive sheet 5 provides a secure mounting location for the chip members 4 so that a resin 6 may be applied thereto. Advantageously, thereafter, grinding and polishing is applied not only to the applied resin but also to the chip members on the back side of side opposite the side at which the electrical connections for the chip members 4 are made. Through this grinding and polishing procedure, the chip has its thickness substantially reduced thereby providing the ability to achieve improved density for the resultant semiconductor products. The temporary adhesive member 5 upon which the chip members 4 are located for application of the resin both between and on the backside of the chips is thereafter removed for subsequent processing and dicing of the individual chips. This unique manufacturing technique has numerous advantages over the prior art techniques. Damage to the chips is reduced while also enabling selection and combination of various undamaged chip members into a common pseudo-wafer. Damage to the chips is reduced not only in the dicing and grinding but also during etching as described in the Specification. The prior art of record provides no teaching or suggestion regarding this advance in the art which reduces the resultant damage to the chip members during manufacturing.

Accordingly, in light of the foregoing, Applicant respectfully requests that the Examiner now withdraw all rejections and allow the claims in the application.

Respectfully submitted,

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Robert J. Depke
HOLLAND & KNIGHT LLC
55 West Monroe Street, Suite 800
Chicago, Illinois 60603
Tel: (312) 422-9050
Attorney for Applicant